AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) An integrated circuit comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

a programmable storage location storing a first temperature limit value, the programmable storage location accessible via an instruction executed by the integrated circuit; and

compare logic coupled to the temperature sensor and the storage location to provide an indication of a comparison between the temperature measurement and the first temperature limit value,

wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value; and

wherein the instruction is assigned a privilege level sufficient to access the programmable storage location.

2. (Canceled)

3. (Previously Presented) The integrated circuit as recited in claim 1 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement indicated by the temperature sensor falls below a programmable second temperature limit value.

4. (Canceled)

5. (Previously Presented) The integrated circuit as recited in claim 1 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, according to a programmable mode of operation that includes at least one of deasserting when the temperature measurement falls below a

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programmable second temperature limit value and deasserting when a control location in the integrated circuit is accessed.

6. (Previously Presented) The integrated circuit as recited in claim 1 wherein the first temperature limit value is a panic value indicating a temperature limit for safe integrated circuit operation.

7. (Previously Presented) The integrated circuit as recited in claim 1 further comprising an addressable storage location coupled to the temperature sensor, the addressable storage location accessible by an instruction executed by the integrated circuit and supplying an indication of the temperature measurement on the integrated circuit.

8. (Previously Presented) The integrated circuit as recited in claim 1 further comprising:
a second output terminal coupled to provide external to the integrated circuit an asserted signal when the temperature measurement indicated by the temperature sensor is above a second temperature limit value.

9. (Original) The integrated circuit as recited in claim 8 further comprising:
a second storage location supplying the second temperature limit value; and
second compare logic coupled to the second storage location and coupled to receive the temperature measurement of the integrated circuit, and wherein the second compare logic generates a second indication of when the temperature measurement of the integrated circuit is above the second temperature limit value.

10. (Original) The integrated circuit as recited in claim 9 further comprising:
a third storage location supplying a third temperature limit value;
third compare logic coupled to the third storage location and coupled to receive the temperature measurement, and wherein the compare logic generates a third indication that the temperature measurement of the integrated circuit is below the third temperature limit value.

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11. (Previously Presented) The integrated circuit as recited in claim 10 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement indicated by the temperature sensor is below the third temperature limit value.

12. (Original) The integrated circuit as recited in claim 1 wherein the integrated circuit is a microprocessor.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Canceled)

24 – 25. (Canceled)

26. (Canceled)

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27. (Canceled)

28. (Canceled)

29. (Canceled)

30 – 33. (Canceled)

34. (Canceled

35. (Canceled)

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (Canceled)

40. (Currently amended) ~~The integrated circuit of claim 1,~~ An integrated circuit comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

a programmable storage location storing a first temperature limit value, the programmable storage location accessible via an instruction executed by the integrated circuit; and

compare logic coupled to the temperature sensor and the storage location to provide an indication of a comparison between the temperature measurement and the first temperature limit value,

wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value; and

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wherein a BIOS includes the instruction.

41. (Currently amended) The integrated circuit of claim [[39]] 40 further comprising the BIOS executable to set addresses for the compare logic and to map the programmable storage location to an input/output space.

42. (Canceled)

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